IN THE CLAIMS

Please amend the claims as follows:

1. (original) A method of manufacturing a trench gate semiconductor device comprising the steps of:

providing a silicon device body having a first major surface, the silicon device body having a drain region of a first conductivity type and a body region over the drain region;

forming a trench extending downwards into the silicon device body from the first major surface, the trench having sidewalls and a base;

etching the silicon at the base of the trench to form porous silicon at the base of the trench; and

thermally oxidising the device to oxidise the porous silicon at the bottom of the trench to form a plug at the base of the trench; and

depositing conductive material within the trench to form a gate.

2. (original) A method according to claim 1 further comprising, after the step of etching the trench, the step of lining the side walls of the trench with dielectric liner for preventing the side

walls becoming porous during the step of forming porous silicon at the bottom of the trench.

3. (original) A method according to claim 1 wherein the step of oxidising the device forms sidewall oxide on the sidewalls of the trench, the method further comprising the steps of etching away the oxide formed on the side wall oxide and of forming the gate oxide by thermal oxidation on the side wall before the step of depositing conductive material within the trench to form a gate.

4. (currently amended) A method according to ~~any preceding claim~~claim 1 wherein the step of forming the trench includes providing a mask on the first major surface defining an opening and etching the trench extending downwards from the first major surface through the opening.

5. (original) A method according to claim 4 wherein the mask is an oxide hard mask.

6. (currently amended) A method according to claim 4~~ or 5~~ wherein the step of etching the silicon at the bottom of the trench to form porous silicon includes dry-etching the bottom of the trench through the same mask used to define the trench.

7. (currently amended) A method according to ~~any preceding claim~~claim 1 further comprising depositing a silicon plug in the trench wherein the step of etching the silicon at the bottom of the trench includes etching the silicon plug.

8. (currently amended) A method according to ~~any preceding claim~~claim 1 further comprising forming a source implant of first conductivity type at the first major surface adjacent to the trench and forming source, gate and drain electrodes attached to the source implant, the gate and the drain region at the bottom of the trench respectively to complete the trench gate semiconductor device.

9. (original) A trench MOSFET comprising:

a drain region of first conductivity type;

a body region over the drain region;

a trench extending from a first major surface through the body region;

source regions of the first conductivity type laterally adjacent to the trench at the first major surface;

thermal gate oxide on the side walls of the trench;

a gate electrode in the trench insulated from the body region by the gate oxide;

characterised by a thick oxide plug formed of oxidised porous silicon at the base of the trench extending into the drain region.

10. (original) A trench MOSFET according to claim 9 wherein the body region is of second conductivity type opposite to the first conductivity type.